Amendments To The Claims

The listing of claims presented below will replace all prior versions, and listings, of claims in the application.

Listing of claims:

1. (**currently amended**) A bit line precharge signal generator for a memory device, the memory device having a plurality of bit line sense amplifier arrays, the bit line precharge signal generator comprising:

a control signal generator for generating a first control signal; and

a plurality of bit line precharge signal drivers being controlled by the first control signal from the control signal generator,

wherein each of the bit line precharge signal drivers applies a second signal to the bit line sense amplifier array which is adjacent to the bit line precharge signal driver**, and**

wherein the plurality of bit line precharge signal drivers are arranged alternately with respect to the plurality of bit line sense amplifier arrays.

2. (**cancelled**)

3. (original) The bit line precharge signal generator according to claim 1, wherein each of the bit line sense amplifier arrays includes a plurality of bit line sense amplifiers, and the second signal is applied to each of the plurality of bit line sense amplifiers.

4. (original) The bit line precharge signal generator according to claim 3, wherein the second signal is a bit line precharge signal, which is necessary for the plurality of bit line sense amplifiers.

5. (original) The bit line precharge signal generator according to claim 3, wherein each of the plurality of bit line sense amplifiers includes:

an amplifier;

a first bit line equalizing transistor arranged at an upper portion of the amplifier;

first bit line isolation transistors arranged between the amplifier and the first bit line equalizing transistor;

second bit line isolation transistors arranged at a lower portion of the amplifier; and

bit line precharge transistors arranged between the amplifier and the second bit line isolation transistors,

wherein the first and second bit line equalizing transistors, and the bit line precharge transistors are driven by the second signal.

6. (new) A bit line precharge signal generator for a memory device having a bit line sense amplifier array comprising:

a control signal generator for generating a bit line precharge enable signal;

a first precharge driver for generating a first precharge signal to precharge the bit line sense amplifier array in response to the bit line precharge enable signal; and

a second precharge driver for generating a second precharge signal to precharge the bit line sense amplifier array in response to the bit line precharge enable signal;

wherein each of the first precharge driver and the second precharge driver is located adjacently to both sides of the bit line sense amplifier array.

7. (new) The bit line precharge signal generator according to claim 6, wherein the first precharge signal includes an upper sense amplifier array precharge signal

controlling an upper part of the sense amplifier array and a lower sense amplifier array precharge signal controlling a lower part of the sense amplifier array.

8. (new) The bit line precharge signal generator according to claim 7, wherein the control signal generator includes a NAND gate receiving both the upper sense amplifier array precharge signal and the lower sense amplifier array precharge signal and a buffer receiving an output from the NAND gate.